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EXAMINER	
HARKNESS, CHARLES A	

ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 10/19/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/640,901	SUDHARSANAN ET AL.	
	Examiner	Art Unit	
	Charles A Harkness	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 July 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-4 and 18-43* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4 and 18-43* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. In view of the amendment to the title, the objection to the specification has been withdrawn.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1-4, 18-21, 23-24, and 27-43 are rejected under 35 U.S.C. 102(e) as being anticipated by Kanakogi et al., U.S. Patent Number 6,609,143 (herein referred to as Kanakogi).

3. Referring to claim 1 Kanakogi has taught a method of executing a single instruction parallel multiply-add function on a processor, the method comprising: providing the processor with an opcode indicating a parallel multiply-add instruction; providing the processor with a first, a second and a third value, wherein each of the values comprises two or more operand components (Kanakogi column 1 lines 24-61 figure 12);

multiplying first operand components of the first and the second values to generate a first intermediate value; multiplying second operand components of the first and the second values to generate a second intermediate value; adding a first operand component of the third value to the first intermediate value to generate a first result value (Kanakogi column 1 lines 24-61 figure 12);

adding a second operand component of the third value to the second intermediate value to generate a second result value; storing the first result value in a first portion of a result location; and storing the second result value in a second portion of the result location (Kanakogi column 1 lines 24-61 figure 12).

4. Referring to claim 2 Kanakogi has taught wherein the first, second and third values are stored in respective source registers of the processor specified by the parallel multiply-add instruction, and the first and the second result values are stored in a destination register of the processor specified by the parallel multiply-add instruction (Kanakogi column 1 lines 24-61 figure 12).

5. Referring to claim 3 Kanakogi has taught the first result value is stored in the high-order bits of the destination register and the second result value is stored in the low-order bits of the destination register (Kanakogi column 1 lines 24-61 figure 12; the instruction would have to indicate which operands to be used in the operation, even if that is by having default registers that are used and preloading the values into those registers).

6. Referring to claim 4 Kanakogi has taught wherein the processor is pipelined and the single instruction is executed with a throughput of one instruction every 2 cycles (Kanakogi column 1 lines 24-61 figure 12; since there is a register in the process, two clock signals would have to be completed before the results were stored).

7. Referring to claim 18 has taught a processor comprising:

a first and second multiplier paths;

a first and second adder paths;

and wherein the processor supports a parallel multiply-add instruction, the parallel multiply add instruction executable to cause the processor to, in parallel, route a first component of a first operand and a first component of a second operand to the first multiplier path and a second component of the first operand and a second component of the second operand to the second multiplier path, in parallel, route output of the first multiplier path and a first component of a third operand to the first adder path, and output of the second multiplier path and a second component of the third operand to the second adder path, and store output of the first adder path at a first location and output of the second adder path at a second location (Kanakogi column 1 lines 24-61 figure 12).

8. Referring to claim 19 has taught wherein the parallel multiply-add instruction operates on either integer or fixed point operands (Kanakogi column 1 lines 24-61 figure 12; the values are in integer format).

9. Referring to claim 20 Kanakogi has taught wherein the results of the parallel multiply-add instruction are saturated (Kanakogi column 6 lines 38-46, figure 2; the extender makes sure the values are extended, or saturated).

10. Referring to claim 21 has taught wherein the processor provides multiple saturation modes (Kanakogi column 6 lines 38-46, figure 2; the extender makes sure the values are extended, or saturated).

11. Referring to claim 23 Kanakogi has taught wherein the processor further supports a parallel averaging instruction, the parallel averaging instruction executable to cause the processor to average a first operand's first component and a second operand's first component, and, in parallel, to average the first operand's second component and the second operand's second

component (Kanakogi column 5 line 64-column 6 line 37, figures 1-4; by using the description Applicant provided to perform averaging operations, Kanakogi performs averages; the full adders feed into the shifters, which operate in parallel after adding the lower half and the upper halves of two operands together).

12. Referring to claim 24 Kanakogi has taught wherein the processor further supports a parallel shift instruction, the parallel shift instruction executable to cause the processor to logically shift a first portion of a first value in accordance with a first portion of a second value, and, in parallel, shift a second portion of the first value in accordance with a second portion of the second value (Kanakogi column 6 lines 38-46, figure 2).

13. Referring to claim 27 Kanakogi has taught a computer program product encoded on one or more machine-readable media, the computer program product comprising: an instruction sequence, the instruction sequence including an instance of a parallel multiply add instruction;

the instance of the parallel multiply add instruction having an at least four operand instruction format, wherein execution of the parallel multiply add instruction causes generation of a first product from a first operand's first component and a second operand's first component, in parallel with generation of a second product from the first operand's second component and the second operand's second component, causes generation of a first sum from the first product and a third operand's first component, in parallel with generation of a second sum from the second product and the third operand's second component, and causes the first sum to be stored in accordance with a fourth operand's first component and the second sum to be stored in accordance with the fourth operand's second component (Kanakogi column 1 lines 24-61 figure 12).

14. Referring to claim 28 Kanakogi has taught wherein the operands include one or more of a fixed-point format and an integer format (Kanakogi column 1 lines 24-61 figure 12; the values are in integer format).

15. Referring to claim 29 Kanakogi has taught wherein the first components correspond to the high order bits of the respective operands and the second components correspond to the low order bits of the respective operands (Kanakogi column 1 lines 24-61 figure 12).

16. Referring to claim 30 Kanakogi has taught an apparatus comprising: a plurality of registers; and means for performing, in response to a single instruction instance, a parallel multiply add operation, the parallel multiply add operation causing generation of a first product and a second product in parallel, and causing generation of a first sum and second sum in parallel, wherein an input value for the first sum includes the first product and an input value for the second sum includes the second product (Kanakogi column 1 lines 24-61 figure 12).

17. Referring to claim 31 Kanakogi has taught further comprising a plurality of multipliers and adders (Kanakogi column 1 lines 24-61 figure 12).

18. Referring to claim 32 Kanakogi has taught wherein the parallel multiply add operation further causes storing of the first sum in a first portion of a first of the plurality of registers and storing of the second sum in a second portion of the first register (Kanakogi column 1 lines 24-61 figure 12).

19. Referring to claim 33 Kanakogi has taught a method of executing an instruction instance comprising: generating a first product and a second product in parallel, wherein the first product is from a first and second value and the second product is from a third and fourth value; and generating a first sum and a second sum in parallel, wherein the first sum is from the first

product and a fifth value and the second sum is from the second product and a sixth value (Kanakogi column 1 lines 24-61 figure 12).

20. Referring to claim 34 Kanakogi has taught wherein the first and third values respectively are first and second portions of a first operand, the second and fourth values respectively are first and second portions of a second operand, and the fifth and sixth values respectively are first and second portions of a third operand (Kanakogi column 1 lines 24-61 figure 12).

21. Referring to claim 35 Kanakogi has taught further comprising storing, in parallel, the first sum in a first location and the second sum in a second location (Kanakogi column 1 lines 24-61 figure 12).

22. Referring to claim 36 Kanakogi has taught wherein the first location is a first portion of a destination register and the second location is a second portion of the destination register (Kanakogi column 1 lines 24-61 figure 12).

23. Referring to claim 37 Kanakogi has taught wherein the instruction instance is executed by a pipelined processor that performs operations for the instruction instance in 2 cycles (Kanakogi column 1 lines 24-61 figure 12; since there is a register in the process, two clock signals would have to be completed before the results were stored).

24. Referring to claim 38 Kanakogi has taught embodied as a computer program product encoded in one or more machine-readable media (Kanakogi column 1 lines 24-61 figure 12).

25. Referring to claim 39 Kanakogi has taught wherein the first store location is a first part of a register and the second store location is a second part of the register (Kanakogi column 1 lines 24-61 figure 12).

26. Referring to claim 40 Kanakogi has taught wherein the first store location is a first register and the second store location is a second register (Kanakogi column 1 lines 24-61 figure 12; the results are split into a high register portion and a low register portion, which act as two separate registers).

27. Referring to claim 41 Kanakogi has taught wherein the first and second multiplier paths are embodied as distinct functional units (Kanakogi column 1 lines 24-61 figure 12).

28. Referring to claim 42 Kanakogi has taught wherein the first and second adder paths are embodied as distinct functional units (Kanakogi column 1 lines 24-61 figure 12).

Referring to claim 43 Kanakogi has taught the processor of claim 23 further comprising: a plurality of adder paths; and a plurality of shifter paths; wherein the parallel averaging instruction, when executed, causes the processor to, route the first operand's first component and the second operand's second component to a first of the plurality of adder paths, and, in parallel, route the first operand's second component and the second operand's second component to a second of the plurality of adder paths; after propagation delay, route output of the first adder path and a one value to a third of the plurality of adder paths, and, in parallel, route output of the second adder path and a one value to fourth of the plurality of adder paths; after propagation delay, route output of the third adder path and a first control value a first of the plurality of shifter paths, and, in parallel, route output of the fourth adder path and a second control value to a second of the plurality of shifter paths (Kanakogi column 5 line 64 column 6 line 37, figures 1-4; the full adders feed into the shifters, which operate in parallel after adding the lower half and the upper halves of two operands together).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

29. Claims 22 and 25-26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kanakogi in view of Oberman U.S. Patent Number 6,490,607 (herein referred to as Oberman).

30. Referring to claim 22 Kanakogi has not taught wherein the processor further supports a conditional pick instruction, the conditional pick instruction executable to cause the processor to compare a first value to zero and to copy either a second value or a third value to a destination location depending on the comparison. Oberman has taught wherein the processor further supports a conditional pick instruction, the conditional pick instruction executable to cause the processor to compare a first value to zero and to copy either a second value or a third value to a destination location depending on the comparison (Oberman figure 14 column 6 lines 3-34; since Oberman employs branching in its system, it would contain the Branch if not equal instruction, where the system compares a given value to zero, and then either branches to another place in the program, or continues on in order, depending on the result, and these two scenarios will alter which value is then placed in the PC register). The use of branching, and branch prediction speeds up the execution of a program by predicting whether the branch will change the next instruction to be processed or not. It would have been obvious to one of ordinary skill in the art at the time of the invention to use branching and branch prediction to speed up the execution of a program in the system.

31. Referring to claim 25 Kanakogi has not taught wherein the processor further supports a parallel power instruction, the parallel power instruction executable to cause the processor to raise a first component of a first operand to a power indicated in a first component of a second operand and, in parallel, raise a second component of a the first operand to a power indicated in a second component of the second operand. Oberman has taught wherein the processor further supports a parallel power instruction, the parallel power instruction executable to cause the processor to raise a first component of a first operand to a power indicated in a first component of a second operand and, in parallel, raise a second component of a the first operand to a power indicated in a second component of the second operand (Oberman column 2 line 64-column 3 line 37). Having these additional features helps the processor for complicated floating point calculations for graphic instructions (Oberman column 2 lines 30-63). Having hardware that can execute a parallel power instruction will significantly speed up the process for graphic execution, and reduce the time needed to complete the program. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to have a system with graphic hardware to speed up the execution of graphic related software.

32. Referring to claim 26 Kanakogi has not taught wherein the processor further supports a parallel reciprocal square root instruction, the parallel reciprocal square root instruction executable to cause the processor to, determine a reciprocal square root of an operand's first component and, in parallel, determine a reciprocal square root of the operand's second component. Oberman has taught wherein the processor further supports a parallel reciprocal square root instruction, the parallel reciprocal square root instruction executable to cause the processor to, determine a reciprocal square root of an operand's first component and, in parallel,

determine a reciprocal square root of the operand's second component (Oberman column 2 line 64-column 3 line 37). Having these additional features helps the processor for complicated floating point calculations for graphic instructions (Oberman column 2 lines 30-63). Having hardware that can execute a reciprocal square root instruction will significantly speed up the process for graphic execution, and reduce the time needed to complete the program. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to have a system with graphic hardware to speed up the execution of graphic related software.

Response to Arguments

33. Applicant's arguments filed 07/16/04 have been fully considered but they are not persuasive.

34. In the remarks, in regard to the rejection of the claims, Applicant argues in essence that:

> "The current patent application receives the benefit of parent application fling dates December 3, 1998 and January 29, 1999...Kanakogi does not qualify as a 102(e) reference against the current patent application."

35. This is not found persuasive. Although the Applicant has submitted for the benefit of parent application rights, in amendment filed 01/30/04, the benefits are for continuation-in-part of co-pending U.S. Application No. 09/204,480, now U.S. Patent Number 6,718,457, and co-pending U.S. Application No. 09/240,977, now U.S. Patent Number 6,341,300, wherein the contents of independent claim 1 lines 4-15 of the instant application have not been disclosed in the parent applications, and therefore is considered new matter. Therefore, the filing date of the instant application will be used as the effective filing date for the claims. The other independent claims of the instant application have similar limitations to claim 1 that have not been disclosed

in the parent application. Therefore the 102 and 103 rejections using Kanakogi are proper and will be maintained. Please see section 201.08 of the MPEP on continuation-in-part.

36. In the remarks, in regard to the rejection of the claims, Applicant argues in essence that:

"Oberman does not disclose or suggest arithmetic instruction that perform operations in parallel."

37. In response to applicant's arguments against the references individually, one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986). Applicant only discusses Oberman and not the combination of the references of the 103 rejection together.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event,

however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Charles A Harkness whose telephone number is 703-305-7579. The examiner can normally be reached on 8Flex.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on 703-305-9712. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Charles Allen Harkness

Examiner

Art Unit 2183

October 14, 2004

EDDIE CHAN
SUPERVISORY PATENT EXAMINER
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